Amendment to the Specification:

At page 1, line 2, please insert the following header and paragraph:

RELATED PATENT DOCUMENTS

This patent application is the national stage filing under 35 U.S.C. 371 of International Application No. PCT/US2004/008141 filed on March 17, 2004 to which benefit is claimed under 35 U.S.C. 365.

At page 5, lines 12-13, please amend the paragraph as follows:

FIG. 2D shows the device of FIG. 2C with the germanium ~~grmanium~~ layer patterned to form germanium device locations on the substrate;

At page 16, lines 23-32, please amend the paragraph at lines 23 and 30 as follows:

FIG. 4A shows a cross-sectional, cut-out view of a silicon wafer 400 coated with an inert-type layer 410 having an array of seed openings 406, 407, 408 and 409 patterned therein, according to another example embodiment of the present invention. The device 400 can be implemented using, for example, one of the germanium crystallization approaches discussed above with the seed openings 406-409 being used to initiate the crystallization of liquefied germanium. Referring to cutout portion 401, seed opening 406 includes a generally rectangular opening extending down to the inert-type layer 410, with sidewalls including exposed sidewalls 460 and 462. ~~461.~~ In one implementation, the device 400 is used to form Silicon-based devices adjacent germanium devices employing the seed openings 406-409.

Amendment to the Specification:

At pages 17-18, lines 22-32 and 1-12 respectively, please amend the paragraph (at page 8, line 7) as follows:

As discussed above, the single-crystal germanium formed in connection with various example embodiments can be used in the formation of a variety of devices. FIG. 5 shows one such device 500 including an insulated gate field-effect transistor (IGFET) having an epitaxially-grown germanium-based active layer 524 in a GeOI structure, according to another example embodiment of the present invention. The IGFET-type device 500 includes an inert-type layer 510 over a bulk substrate 505 and the active germanium-based layer 524 on the inert-type layer. The active germanium-based layer 524 is grown using one or more of the above-discussed approaches, with patterning used to form the end device as shown. Growth of the active germanium-based layer 524 involves the initiation of crystallization at a seed location 512, with a first stage of crystalline growth in region 525 of the germanium-based layer extending upward. This first region 525 generally includes defects associated with a lattice mismatch at an interface between the germanium-based layer 524 and the bulk substrate 505 at the seed location 512. Upon a change in direction of growth to a generally horizontal direction in region 526 of the germanium-based layer 524, defects due to the lattice mismatch are substantially terminated. Continuing propagation of a crystalline front in the generally horizontal direction in region 526 forms substantially single-crystal germanium. A gate dielectric layer 552 ~~522~~ in the single-crystal germanium region 526 separates a channel region 564 from a gate electrode 550. Source/drain regions 560 and 562 are also in the single-crystal germanium region 526 and are electrically coupled in a current-passing mode when the channel region 564 is switched into a current-passing state via a signal applied to the gate electrode 550. In some implementations, portions of the active germanium-based layer 524 near the seed location 512 are removed.